EXHIBIT H

Time-Critical Software Deceleration in an FCCM

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Authors Phil James-Roxby Xilinx Research Labs, Longmont, CO, USA
Gordon Brebner Xilinx Research Labs, San Jose, CA, USA
Dennis Bemmann Humboldt University, Berlin, Germany

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ABSTRACT

In this paper, we explore two important latency issues associated with using an embedded processor as an assistant to programmable logic within a logic-centric system implemented ona platform FPGA. The context is that of the 'software decelerator' - a term introduced by the authors in 2003 to describe a logic-centric counterpart of the familiar hardware accelerator.We first focus on minimizing latency in the logic-processor interface, introducing an efficient interrupt-driven control mechanism. Then, in the context of a case study on packet address lookup, we focus on minimizing latency in memory interfaces, using the processor's hardware cache mechanism for assistance.

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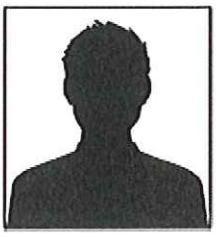
Collaborative Colleagues:

Phil James-Roxby: colleagues

Gordon Brebner: colleagues
Dennis Bemmann: colleagues



Dennis Bemmann

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Authors:
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Affiliation history
· Humboldt-Universität zu Berlin

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